HC24GB Low Cost 2.4GHz Radio Transceiver

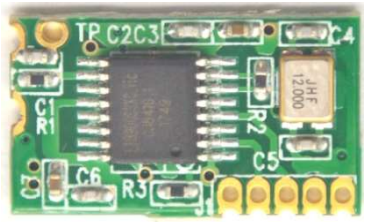
FEATURES

* Complete 2.4 GHz radio transceiver includes fully integrated RF PLL and channel filtering
* Supports Frequency-Hopping Spread Spectrum
* Supports SPI and I^2C bus interface
* Built-in smart auto-acknowledge Tx/Rx protocol simplifies usage
* Packet data rate 1 Mbps over-the-air
* FIFO flag signal permits continuous streaming data at 1 Mbps over-the-air
* Power management for minimizing current consumption
* Digital readout of RSSI and temperature

RoHS Lead Free

Application

* Remote controls
* Wireless keyboards and mice
* Proprietary Wireless Networks
* Home automation
* Commercial and industrial short-range wireless
* Wireless voice, VoIP, Cordless headsets
* Robotics and machine connectivity



ENERAL DESCRIPTION

The HC24GB is a low-cost, fully integrated CMOS RF transceiver module, GFSK data modem, and packet framer, optimized for use in the 2.4GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

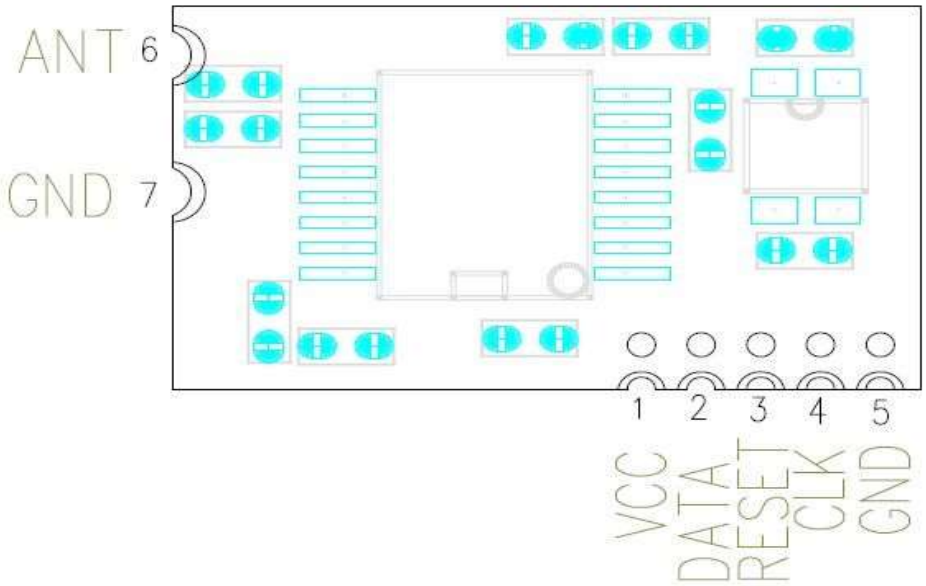
The HC24GB transmits GFSK data at approximately 1 dBm output power. The low-IF receiver architecture produces good selectivity, with sensitivity down to approx. -87 dBm. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

The digital baseband interface can be either 4-wire SPI or 2-wire I2C-bus. Three additional pins are available for optional reset and buffer control.

For extended battery life, power consumption is minimized all key areas. A sleep mode is available to reduce standby current consumption to just 1 uA typ. while preserving register settings.

1. PIN DESCRIPTION



PIN No.	Name	I/O/P	Description
1	VCC	P	Module Power supply Positive
2	RESET	I	Module Hardware Reset, low pulse active
3	SDA	I/O	Module I2C serial DATA.
4	SCL	I	Module I2C serial CLOCK
5	GND	P	Power negative,ground
6	ANT	O	Module antenna
7	GND	P	Module Power supply negative, ground.

P: is ower supply

2. Absolute Maximum Ratings

Table 1. Absolute Maximum Rating

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Temp.	T_{OP}	-40		+85	ºC
Storage Temp.	$T_{STORAGE}$	-55		+125	ºC
LDO_VDD, VDD_IO Voltage	V_{IN_MAX}			+3.7	VDC
VDD pins	VDD_MAX			+2.5	
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z0=50Ω)	VSWROUT			10:1	VSWR

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

3. Electrical Characteristics

Table 2. Electrical Characteristics

The following specifications are guaranteed for TA = 25 C, LDO_VDD= VDD_IO = 3.3 VDC, unless otherwise noted.

Parameter	Symbol	MIN	TYP	MAX	Units	Test Condition and Notes
Supply Voltage						
DC power supply voltage range		1.9		3.6	VDC`	Input to VDD_IO and LDO_VDD pins.
Current Consumption						
Current Consumption - TX	IDD_TXH		18		mA	POUT = high power setting
	IDD_TXL		12		mA	POUT = low power setting
Current Consumption - RX	IDD_RX		17		mA	
Current Consumption –IDLE	IDD_IDLE1		1.4		mA	Configured for BRCLK output running.
	IDD_IDLE2		1.1		mA	Configured for BRCLK output OFF.
Current Consumption - SLEEP	IDD_SLP		1		uA	
Digital Inputs						
Logic input high	VIH	0.8 VDD_IN		1.2 VDD_IN	V	
Logic input low	VIL	0		0.8	V	
Input Capacitance	C_IN			10	pF	
Input Leakage Current	I_LEAK_IN			10	uA	
Digital Outputs						
Logic output high	VOH	0.8 VDD_IN		VDD_IN	V	
Logic output low	VOL			0.4	V	
Output Capacitance	C_OUT			10	pF	
Output Leakage Current	I_LEAK_OUT			10	uA	
Rise/Fall Time (SPI)	T_RISE_OUT			5	nS	
Clock Signals						
CLK rise, fall time (SPI)	Tr_spi			25	nS	Requirement for error-free register reading, writing.
CLK frequency range (SPI)	FSPI	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	F_OP	2400		2482	MHz	
Antenna port mismatch	VSWR_I		<2:1		VSWR	Receive mode.
(Z0=50Ω)	VSWR_O		<2:1		VSWR	Transmit mode.

Parameter	Symbol	MIN	TYP	MAX	Unis	Test Condition and Notes
Receive Section						Measured using 50 Ohm balun. For BER ≤ 0.1%:
Receiver sensitivity			-87		dBm	FEC off.
Maximum useable signal		-20	1		dBm	
Data (Symbol) rate	Ts		1		us	
Min. Carrier/Interference ratio						For BER ≤ 0.1%
Co-Channel Interference	CI_cochannel		+9		dB	-60 dBm desired signal.
Adjacent Ch. Interference, 1MHz offset	CI_1		+6		dB	-60 dBm desired signal.
Adjacent Ch. Interference, 2MHz offset	CI_2		-12		dB	-60 dBm desired signal.
Adjacent Ch. Interference, 3MHz offset	CI_3		-24		dB	-67 dBm desired signal.
Out-of-Band Blocking For additional test conditions, see footnote1.	OBB_1	-10			dBm	30 MHz to 2000 MHz
	OBB_2	-27			dBm	2000 MHz to 2400 MHz
	OBB_3	-27			dBm	2500 MHz to 3000 MHz
	OBB_4	-10			dBm	3000 MHz to 12.75 GHz
						Meas. with ACX BF2520 ceramic filter 2 on ant. pin . Desired sig. -67 dBm, BER ≤ 0.1%.
Transmit Section						Measured using 50 Ohm balun3:
RF Output Power	PAV			6		POUT= maximum output power Reg09=0x4000
			2		dBm	POUT = nominal output power, Reg09=0x1840
		-17				POUT=minimum output power,Reg09=1FC0
Second harmonic			-50		dBm	Conducted to ANT pin.
Third harmonic			-50		dBm	Conducted to ANT pin.
Modulation Characteristics						
Peak FM Deviation 00001111 pattern	Δf1avg		280		kHz	
Peak FM Deviation 01010101 pattern	Δf2max		225		kHz	
In-Band Spurious Emission						
2MHz offset	IBS_2			-40	dBm	
>3MHz offset	IBS_3			-60	dBm	
Out-of-Band Spurious Emission, Operation	OBS_O_1		< -60	-36	dBm	30 MHz ~ 1 GHz
	OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal and harmonics.
	OBS_O_3		< -60	-47	dBm	1.8 GHz ~ 1.9 GHz
	OBS_O_4		< -65	-47	dBm	5.15 GHz ~ 5.3 GHz

Note:

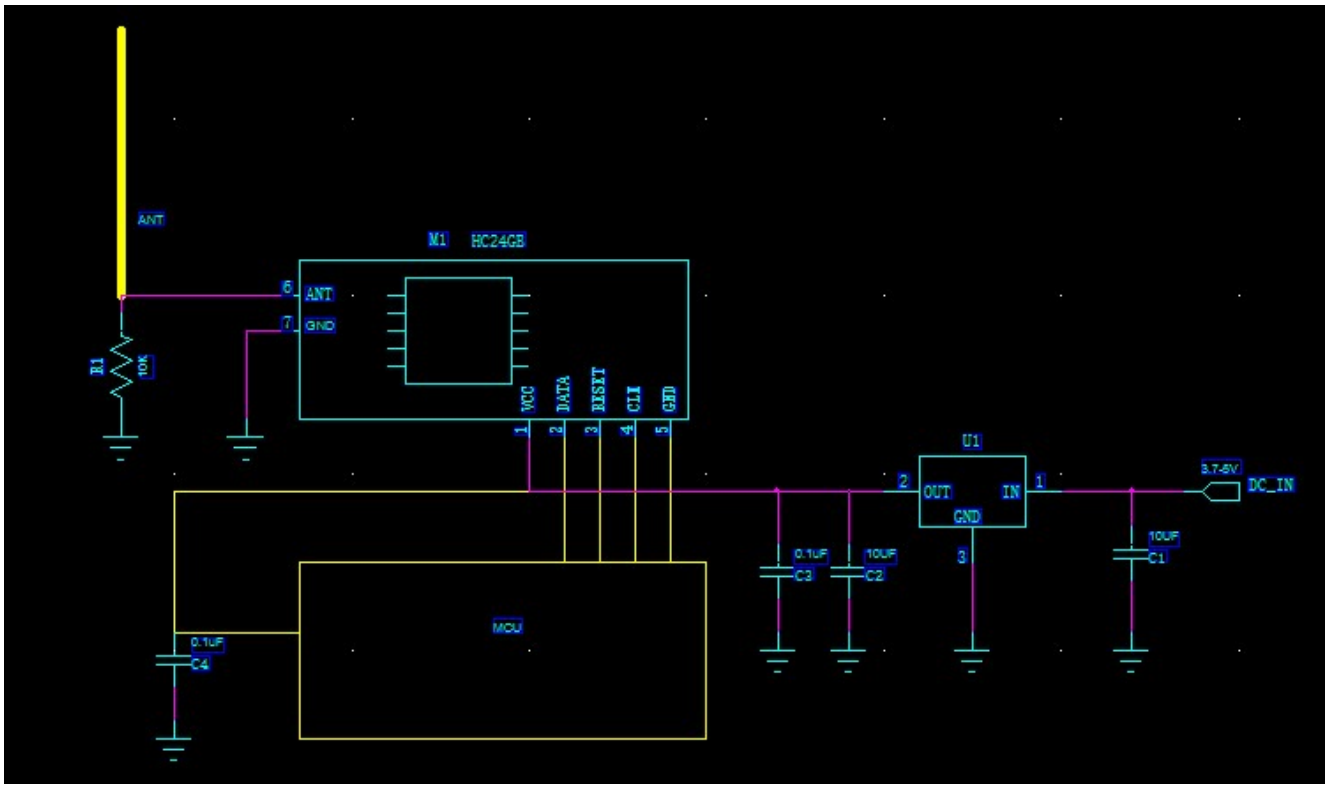
1. ***The test is run at one midband frequency, typically 2460 MHz. With blocking frequency swept in 1 MHz steps, up to 24 exception frequencies are allowed. Of these, no more than 5 shall persist with blocking signal reduced to -50dBm. For blocking frequencies below desired receive frequency, in-band harmonics of the out-of-band blocking signal are the most frequent cause of failure, so be sure blocking signal has adequate harmonic filtering.***
2. ***In some applications, this filter may be incorporated into the antenna, or be approximated by the effective antenna bandwidth.***
3. ***Transmit power measurement is corrected for insertion loss of Balun, in order to indicate the transmit power at the IC pin***

Parameter	Symbol	MIN	TYP	MAX	Unit	Test Condition and Notes	
RF VCO and PLL Section							
Typical PLL lock range	FLOCK	2366		2516	MHz		
Tx, Rx Frequency Tolerance			--		ppm	Same as XTAL pins frequency tolerance	
Channel (Step) Size			1		MHz		
SSB Phase Noise			≤ -95		dBc/Hz	550kHz offset	
			≤ -115		dBc/Hz	2MHz offset	
Crystal oscillator freq. range (Reference Frequency)			12.000		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.			±20		ppm	See Register 27 description. Amount of pull depends on crystal spec. and operating point.	
RF PLL Settling Time	THOP		75	150	uS	Settle to within 30 kHz of final value.	
Spurious Emissions	OBS_1		< -75	-57	dBm	30 MHz ~ 1 GHz	IDLE state, Synthesizer and VCO ON.
	OBS_2		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	Vdo		0.17	0.5	V	Measured during Receive sta	

4. Typical Application

2.4 GHz Wireless Data Transceiver with IIC

Figure 1. HC24GB Typical Application Schematic



5. IIC Interface

5.1. I2C Command Format

Figure 4. Example I2C Data Transfers

I2C sequence package format of HC24G: (see software routines for ACK,NACK, STOP, and I2C sequence, speed, etc.)

Master write 1 or more data byte to HC24G FIFO register:

Start	Device_addr[6:0]	W	A	Byte_addr[7:0]	A	Data[7:0]	A	……	A	Data[7:0]	A	stop

Master writes 1 byte to HC24G to specify FIFO register, then reads one or more bytes from HC24G FIFO:

Star	Devide_addr[6:0]	W	A	Byte_addr[7:0]	A	Sr	Devide_addr[6:0]	R	A	Data[7:0]	A	……	A	Data[7:0]	A	stop

Master may continue reading HC24G FIFO:

Start	Device_addr[6:0]	R	A	Data[7:0]	A	Data[7:0]	A	……	A	Data[7:0]	A	stop

A: ACK
W: Write
R: Read

Note: please use logic analyzer to capture data during development. To verify the communication, the software first reads the register data of the module, if it can read, the description Control is up.

5.2. I2C Supported Features

Table 3. I2C Supported Feature List

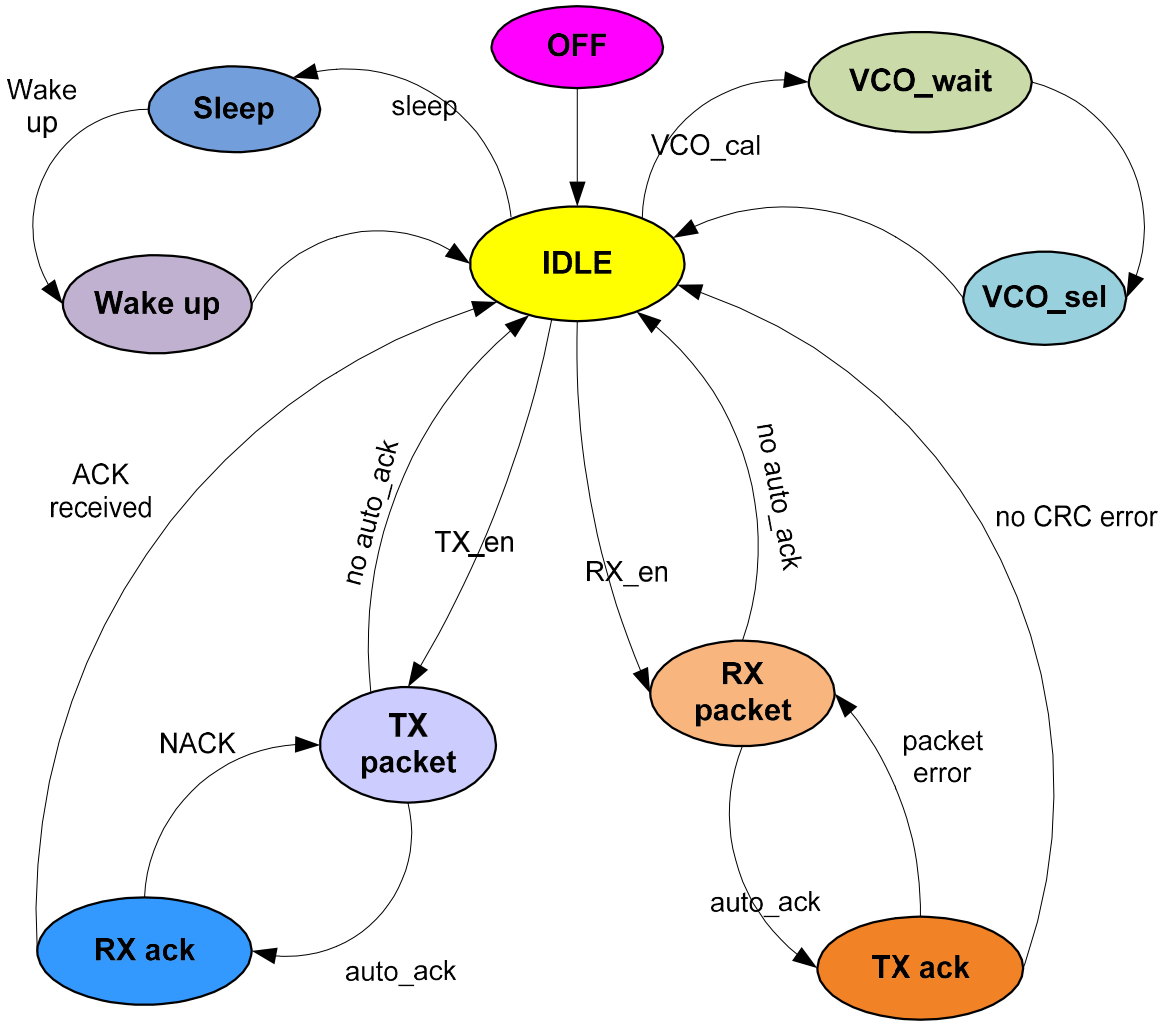
I2C device Slave Mode Optional Feature List	Support?
Standard-mode – 100 kbps	Yes
Fast-mode – 400 kbps	Yes
Fast-mode Plus – 1000 kbps	Yes
High-speed mode – 3200 kbps	No
Clock Stretching	No
10-bit slave address	No
general call address	No
software reset	No
device ID	No

5.3. I2C Device Address

In I2C mode, the HC24GB responds to the following device address:

A6	A5	A4	A3	A2	A1	A0	R/W
0	Determined by bonding pad jumper. QFN packaged parts: Standard is '1'. Special order option is '0'. Bare Die: can be bonded however required.	Determined by bonding pad jumper. QFN packaged parts: As determined by pin 15, MOSI/A4. Bare Die: can be bonded however required.	1	0	0	0	Read=1 Write=0

6. Top Level State Diagram



7. Register Information

The following registers are accessed using I2C serial interface protocol.

Some of the internal registers and bit fields are not intended for end-user adjustment. Such registers are not described herein, and should not be altered from the factory-recommended value.

7.1. Register 3 – Read only

Table 4. Register 3 information

Bit No.	Bit Name	Description
15:13	(Reserved)	(Reserved)
12	RF_SYNTH_LOCK	Indicates the phase lock status of RF synthesizer. 1: Locked. 0: Unlocked.
11:0	(Reserved)	(Reserved)

7.2. Register 6 – Read only

Table 5. Register 6 information

Bit No.	Bit Name	Description
15:10	RAW_RSSI[5:0]	Indicate 4-bit raw RSSI values from analog circuit.
9:0	(Reserved)	(Reserved)

7.3. Register 7

Table 6. Register 7 information

Bit No.	Bit Name	Description
15:9	(Reserved)	(Reserved)
8	TX_EN	Initiate the Transmit Sequence for state machine control. Note that TX_EN and RX_EN cannot be “HIGH” at the same time.
7	RX_EN	Initiate the Receive Sequence for state machine control. Note that TX_EN and RX_EN cannot be “HIGH” at the same time.
6:0	RF_PLL_CH_NO [6:0]	This will be the 7 bit RF channel number. The on-air frequency will be: f = 2402 + RF_PLL_CH_NO.

7.4. Register 9

Table 7. Register 9 information

Bit No.	Bit Name	Description
15:12	PA_PWCTR[3:0]	PA current control
11	(Reserved)	(Reserved)
10:7	PA_GN[3:0]	4-bit power amplifier gain setting.
6:0	(Reserved)	(Reserved)

7.5. Register 10

Table 8. Register 10 information

Bit No.	Bit Name	Description
15:1	(Reserved)	(Reserved)
0	XTAL_OSC_EN	1: Enable crystal oscillator gain block. 0: Disable crystal oscillator gain block.

7.6. Register 11

Table 9. Register 11 information

Bit No.	Bit Name	Description
15:9	(Reserved)	(Reserved)
8	RSSI_PDN	1: Power down RSSI. 0: RSSI operates normally.
7:0	(Reserved)	(Reserved)

7.7. Register 23

Table 10. Register 23 information

Bit No.	Bit Name	Description
15:3	(Reserved)	(Reserved)
2	TxRx_VCO_CAL_EN	1: Calibrate VCO before each and every Tx/Rx enable. 0: Do not calibrate VCO before each and every Tx/Rx enable.
1:0	(Reserved)	(Reserved)

7.8. Register 27

Table 11. Register 27 information

Bit No.	Bit Name	Description
15:6	(Reserved)	(Reserved)
5:0	XI_trim[5:0]	Crystal frequency trim adjust.

7.9. Register 29 – Read only

Table 12. Register 29 information

Bit No.	Bit Name	Description
15:8	(Reserved)	(Reserved)
7:4	RF_VER_ID [3:0]	This field is used to identify minor RF revisions to the design.
3	(Reserved)	(Reserved)
2:0	Digital version	This field is used to identify minor digital revisions to the design.

7.10. Register 30 – Read only

Table 13. Register 30 information

Bit No.	Bit Name	Description
15:0	ID_CODE_L [15:0]	Lower bits of JEDEC JEP106-K Manufacture's ID code, containing manufacturer, part number, and version. The LSB is always "1".

7.11. Register 31 – Read only

Table 14. Register 31 information

Bit No.	Bit Name	Description
15:12	RF_CODE_ID	JEDEC JEP106-K revision level.
11:0	ID_CODE_M [31:16]	Upper bits of Manufacture's ID code.

7.12. Register 32

Table 15. Register 32 information

Bit	Name	R/W	Description	default
15:13	PREAMBLE_LEN	R/W	000: 1byte, 001: 2bytes, 010: 3 bytes, … 111: 8 bytes	010B
12:11	SYNCWORD_LEN	R/W	11: 64 bits {Reg39[15:0],Reg38[15:0],Reg37[15:0],Reg36[15:0]} 10: 48bits, {Reg39[15:0],Reg38[15:0],Reg36[15:0]} 01: 32bits, {Reg39[15:0],Reg36[15:0] 00: 16 bits,{Reg36[15:0]}	11B
10:8	TRAILER_LEN	R/W	000: 4 bits, 001: 6bits, 010: 8 bits, 011: 10 bits …. 111: 18 bits	000B
7:6	DATA_PACKET_TYPE	R/W	00: NRZ law data 01: Manchester data type 10: 8bit/10bit line code 11: Interleave data type	00B
5:4	FEC_TYPE	R/W	00: No FEC 01: FEC13 10: FEC23 11: reserved	00B

Bit	Name	R/W	Description	default
3:1	BRCLK_SEL	R/W	Selects output clock signal to BRCLK pin: 3'b000: keep low 3'b001: crystal buffer out 3'b010: crystal divided by 2 3'b011: crystal divided by 4 3'b100: crystal divided by 8 3'b101: TXCLK 1 MHz 3'b110: APLL_CLK (12 MHz during Tx, Rx) 3'b111: keep low	011B
0	(Reserved)	W/R	(Reserved)	0B

7.13. Register 33

Table 16. Register 33 information

Bit	Name	R/W	Description	default
15-8	VCO_ON_DELAY_CNT[7:0]	R/W	After set TX or RX wait delay timer for internal VCO setting time. Each time increment is 1 uS.	63H
7-6	TX_PA_OFF_DELAY[1:0]	R/W	Set PA off after PA_OFF command, 1 represents 1us, base is 4us	00B
5:0	TX_PA_ON_DELAY[5:0]	R/W	After set VCO_ON, it will wait this timer , than internal PA fully on,	07H

7.14. Register 34

Table 17. Register 34 information

Bit	Name	R/W	Description	default
15	Bpktctl_direct	R/W	When direct mode, it is used control PA on at TX and wide/narrow mode control at RX	0B
14-8	TX_CW_DLY[6:0]	R/W	Transmit CW modulation data at before transmit data, after PA on, continue TX CW mode time.	03H
7-6	Reserved	R/W		0B
5:0	TX_SW_ON_DELAY[5:0]	R/W	Set VCO_ON, wait this timer, internal TW switch turn on, 1 represents 1us	0BH

7.15. Register 35

Table 18. Register 35 informatio

Bit	Name	R/W	Description	default
15	POWER_DOWN	W	1: First set crystal off, then set LDO low-power mode (register values will be lost). 0: Leave power on.	0B
14	SLEEP_MODE	W	1: Enter SLEEP state (set crystal gain block to off. Keep LDO regulator on (register values will be preserved). Wakeup begins when SPI_SS goes low. This will restart the on-chip clock oscillator to begin normal operation. 0: Normal (IDLE) state.	0B
13	(Reserved)		(Reserved)	
12	BRCLK_ON_SLEEP	R/W	1: crystal running at sleep mode. Draws more current but enables fast wakeup. 0: crystal stops during sleep mode. Saves current but takes longer to wake up.	1B
11:8	RE-TRANSMIT_TIMES	R/W	Max. re-transmit packet attempts when auto_ack function is enabled.	3H
7	MISO_TRI_OPT	R/W	1: MISO stays low-Z even when SPI_SS=1. 0: MISO is tri-state when SPI_SS=1.	0B
6:0	SCRAMBLE_DATA	R/W	Whitening seed for data scramble. Must be set the same at both ends of radio link (Tx and Rx).	00H

7.16. Register 36

Table 19. Register 36 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[15:0]	R/W	LSB bits of sync word is sent first.	0000H

7.17. Register 37

Table 20. Register 37 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[31:16]	R/W	LSB bits of sync word is sent first.	0000H

7.18. Register 38

Table 21. Register 38 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[47:32]	R/W	LSB bits of sync word is sent first.	0000H

7.19. Register 39

Table 22. Register 39 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[63:48]	R/W	LSB bits of sync word is sent first.	0000H

7.20. Register 40

Table 23. Register 40 information

Bit	Name	R/W	Description	default
15:11	FIFO_EMPTY_THRESHOLD	R/W		00100B
10:6	FIFO_FULL_THRESHOLD	R/W		00100B
5:0	SYNCWORD_THRESHOLD	R/W	The minimum allowable error bits of SYNCWORD, 07 means 6 bits，01 means 0 bit	07H

7.21. Register 41

Table 24. Register 41 information

Bit	Name	R/W	Description	default
15	CRC_ON	R/W	1: CRC on. 0: CRC off.	1B
14	SCRAMBLE_ON	R/W	Removes long patterns of continuous 0 or 1 in transmit data. Automatically restores original unscrambled data on receive. 1: scramble on. 0: scramble off.	0B
13	PACK_LENGTH_EN	R/W	1: HC24GB regards first byte of payload as packet length descriptor byte.	1B
12	FW_TERM_TX	R/W	1: When FIFO write point equals read point, LT8900 will terminate TX when FW handle packet length. 0: FW (MCU) handles length and terminates TX.	1B

Bit	Name	R/W	Description	default
11	AUTO_ACK	R/W	1: After receiving data, automatically send ACK/NACK. 0: After receive, do not send ACK or NACK; just go to IDLE.	1B
10	PKT_FIFO_POLARITY	R/W	1: PKT flag, FIFO flag Active low. 0: Active high	0B
9:8	(Reserved)	R/W	(Reserved)	00B
7:0	CRC_INITIAL_DATA	R/W	Initialization constant for CRC calculation.	00H

7.22. Register 42

Table 25. Register 42 information

Bit	Name	R/W	Description	default
15:10	SCAN_RSSI_CH_NO	R./W	Number of consecutive channels to scan for RSSI value. RSSI result of each channel is returned in FIFO registers.	00H
9:8	(Reserved)	R/W	(Reserved)	01B
7:0	Rx_ACK_TIME[7:0]	R/W	Wait RX_ack ID timer setting. 1 represents 1us	6BH

7.23. Register 43

Table 26. Register 43 information

Bit	Name	R/W	Description	default
15	SCAN_RSSI_EN	R./W	1: Start scan_RSSI process.	0B
14:8	SCAN_STRT_CH_OFFST[6:0]	R/W	Normally an RSSI scan would start at 2402 MHz (channel 0). This field introduces a starting offset. EXAMPLE: If offset= +10, Starting channel will be 2412 MHz (ch. 10).	01B
7:0	WAIT_RSSI_SCAN_TIM[7:0]	R/W	Set VCO & SYN setting time when scan different channel RSSI	6BH

7.24. Register 48 – Read only

Table 27. Register 48 information

Bit	Name	R/W	Description	default
15	CRC_ERROR	R	Received CRC error	
14	FEC23_ERROR	R	Indicate FEC23 error	
13:8	FRAMER_ST	R	Framer status	
7	SYNCWORD_RECV	R	1: syncword received, it is just available in receive status, After out receive status, always keep '0'.	
6	PKT_FLAG	R	PKT flag indication	
5	FIFO_FLAG	R	FIFO flag indication	
4:0	(Reserved)	R	(Reserved)	

7.25. Register 50

Table 30. Register 50 information

Bit	Name	R/W	Description	default
15:0	TXRX_FIFO_REG	R/W	For MCU read/write data between the FIFO. Reading this register removes data from FIFO; Writing to this register adds data to FIFO. Note: FW (MCU) access to FIFO is byte-by-byte.	00H

7.26. Register 52

Table 31. Register 51 information

Bit	Name	R/W	Description	default
15	CLR_W_PTR	W	1: clear TX FIFO point to 0 when write this bit to "1". It is not available in RX status.	0B
14	(Reserved)	W		
13:8	FIFO_WR_PTR	R	FIFO write pointer.	
7	CLR_R_PTR	W	1: clear RX FIFO point to 0 when write this bit to "1". It is not available in TX status.	0B
6	(Reserved)			
5:0	FIFO_RD_PTR	R	FIFO read pointer (number of bytes to be read by MCU).	

8. Recommended Register Values

The following register values are recommended for most typical applications. Some changes may be required depending on application.

Table 32. Recommended Register Values

Register number	Power-up reset value (hex)	Recommended value for many applications (hex)	Notes
0	6fef	6fef	
1	5681	5681	
2	6619	6617	
4	5447	9cc9	
5	f000	6637	
7	0030	0030	Use for setting RF frequency, and to start/stop Tx/Rx packets.
8	71af	6c90	
9	3000	1840	Sets Tx power level
10	7ffd	7ffd	Crystal osc. enabled.
11	4008	0008	RSSI enabled.
12	0000	0000	
13	4855	48bd	
22	c0ff	00ff	
23	8005	8005	Calibrate VCO before each and every Tx/Rx.
24	307b	0067	
25	1659	1659	
26	1833	19e0	
27	9100	1200	No crystal trim.
28	1800	1800	
29	00x0	read-only	Stores p/n, version information.
30	f413	read-only	Stores p/n, version information.
31	1002	read-only	Stores p/n, version information.
32	1806	1806	Packet data type: NRZ, no FEC, BRCLK=12 div. by 4= 3MHz
33	6307	3ff0	Configures packet sequencing.
34	030b	3000	Configures packet sequencing.
35	1300	0380	AutoAck max Tx retries = 3
36	0000	Choose unique sync words for each over-the-air network.	Similar to a MAC address.
37	0000		
38	0000		
39	0000		
40	2107	2107	Configure FIFO flag, sync threshold.
41	b800	b000	CRC on. SCRAMBLE off. 1st byte is packet length.
42	fd6b	fdb0	
43	000f	000f	Configure scan_rssi.

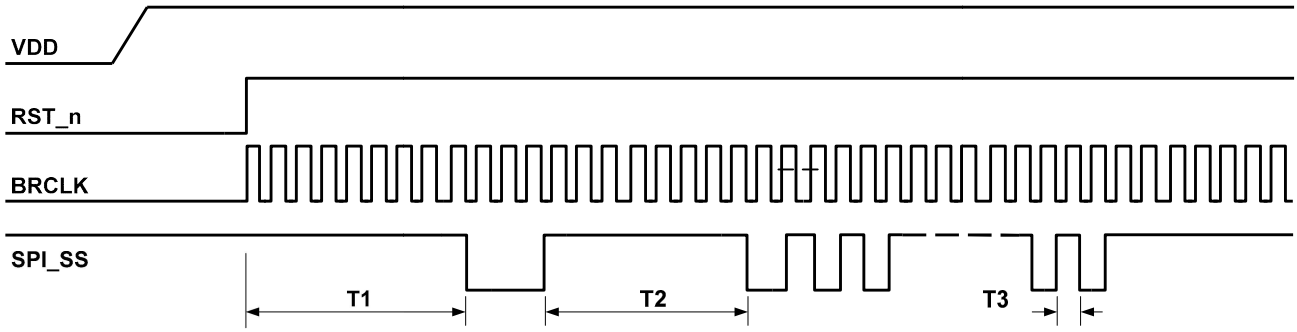
9. Usage Notes

The HC24GB Low-Cost RF Transceiver module can be used to add wireless capability to many applications. The following notes are intended to answer common questions regarding the HC24GB.

9.1. Power On and Register Initialization Sequence

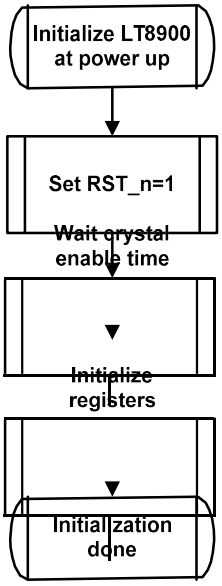
Figure below shows the timing diagram of power-on sequence after VDD is ready.

Figure 5. Power on and register programming sequence



1. After VDD power is ready, make sure to have valid reset on pin RST_n, which is active-low.
2. After RST_n =1, BRCLK will be running at 12MHz clock.
3. Wait T1 (1 to 5 ms) for crystal oscillator to stabilize, then MCU/application can perform register initialization.
4. After register initialization, LT8900 is ready to transmit or receive.

Figure 6. Initialization flowchart

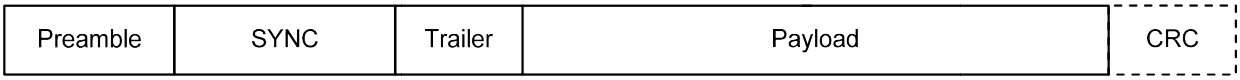


9.2. Enter Sleep and Wake-Up

When MCU writes HC24GB register to enter sleep mode and pulls IIC_SS back to high, HC24GB will enter sleep state where the current consumption is extremely low. When IIC_SS is pulled low, HC24GB will automatically wake up from sleep state. MCU needs to keep SPI_SS low a certain time (the time required for RFIC crystal to be stabilized) before driving IIC_CLK and SPI data.

9.3. Packet Data Structure

Each over-the-air HC24GB packet is structured as follows:



* Preamble: 1~8 bytes, programmable.
* SYNC: 16/32/48/64 bits, programmable as device syncword.
* Trailer: 4~18 bits, programmable.
* Payload: TX/RX data. There are 4 data types:
  - Raw data
  - 8 bit / 10 bit line code
  - Manchester
  - Interleave with FEC option
* CRC: 16-bit CRC is optional.

9.4. FIFO Pointer Clear

For transmit, it is required to clear FIFO write pointer before application writes data to FIFO for transmit. This is accomplished by writing '0' to Register 52[15].

After receiving a packet, the read pointer will indicate how many bytes of receive data are waiting in FIFO buffer, waiting to be read by user MCU or application.

FIFO write pointer will automatically be cleared when receiver receives SYNC.

FIFO read pointer will automatically be cleared when receiver receives SYNC, or after transmitting SYNC in transmit mode.

9.5. Packet Payload Length

HC24GB provides two ways to handle TX/RX packet length. If Register 41[13]= 1, the HC24GB internal framer will detect packet length based on the value of the 1st payload byte. If Register 41[13]= 0, the 1st byte of the payload has no particular meaning, and packet length is determined by either TX FIFO running empty, or TX_EN bit cleared. See table below:

Table 33. Packet Payload Length

Register 41[13] PACK_LENGTH_EN	Register 41[12] FW_TERM_TX	
0 (MCU/application handles packet length)	0	Transmit stops only when Register 7 TX_EN= 0. See page 31 for details. Receive stops only when Register 7 RX_EN= 0. See page 33 for details.
	1	Transmit automatically stops whenever FIFO runs empty. Receive stops only when Register 7 RX_EN= 0. See page 29 for details.
1 (LT8900 framer handles packet length)	x (don't care)	1st byte of payload is regarded as packet length, 0 to 255 bytes. Transmit automatically stops when all 0 to 255 bytes are transmitted. See page 25 for details.

Detailed timing diagrams are shown below.

All timing diagrams show active-high for PKT and FIFO flags. Active-low is also available via Register 41[10] setting.

9.6. Framer handles packet length

Framer of HC24GB will handle packet length by setting Register 41[13]=1. The first byte of payload is regarded as packet length (this length byte is not counted in the packet length). Maximum allowed packet length is 255 bytes. Framer will handle Tx/Rx start and stop.

9.6.1. Transmit Timing

Tx timing diagram is shown below. After MCU writes Register 7[8]=1 and selects transmit channel (refer to Register 7 definition), the framer will automatically generate the packet using payload data from FIFO. MCU needs to fill in transmit data before framer sends trailer bits.

If packet length exceeds FIFO length, the MCU will need to write FIFO data multiple times. FIFO flag indicates whether FIFO is empty in transmit state or not.

Figure 7. Tx Timing Diagram when Register 41[13]= 1 (Framer Handles Packet Length).

PKT and FIFO flags are Active High

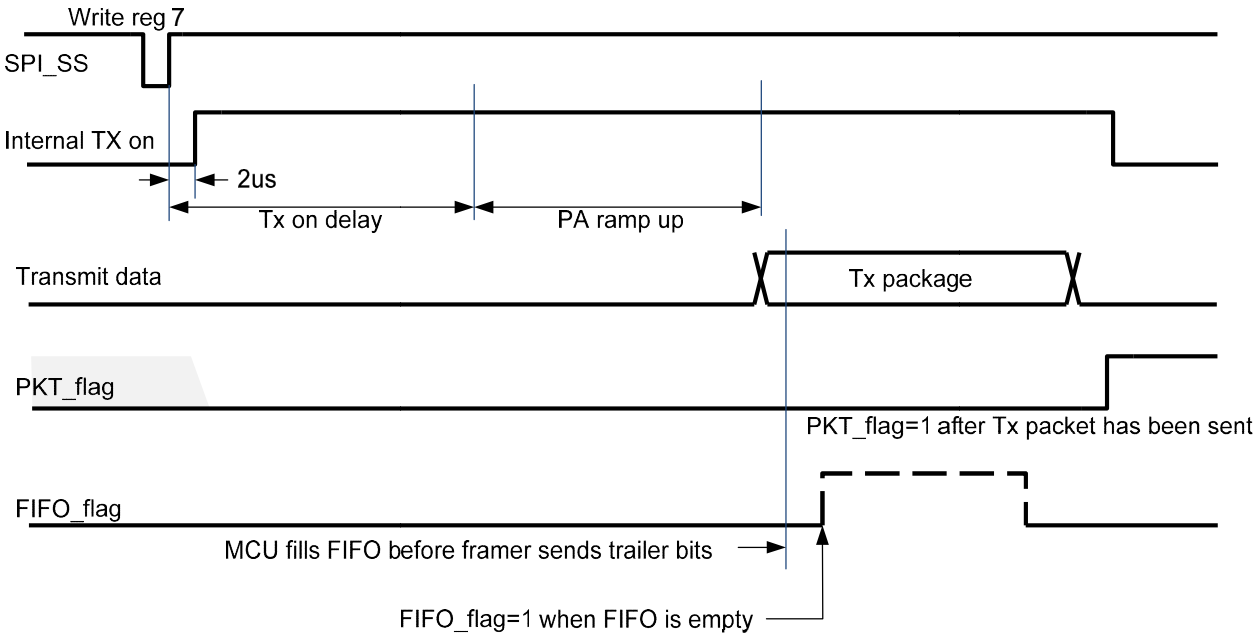
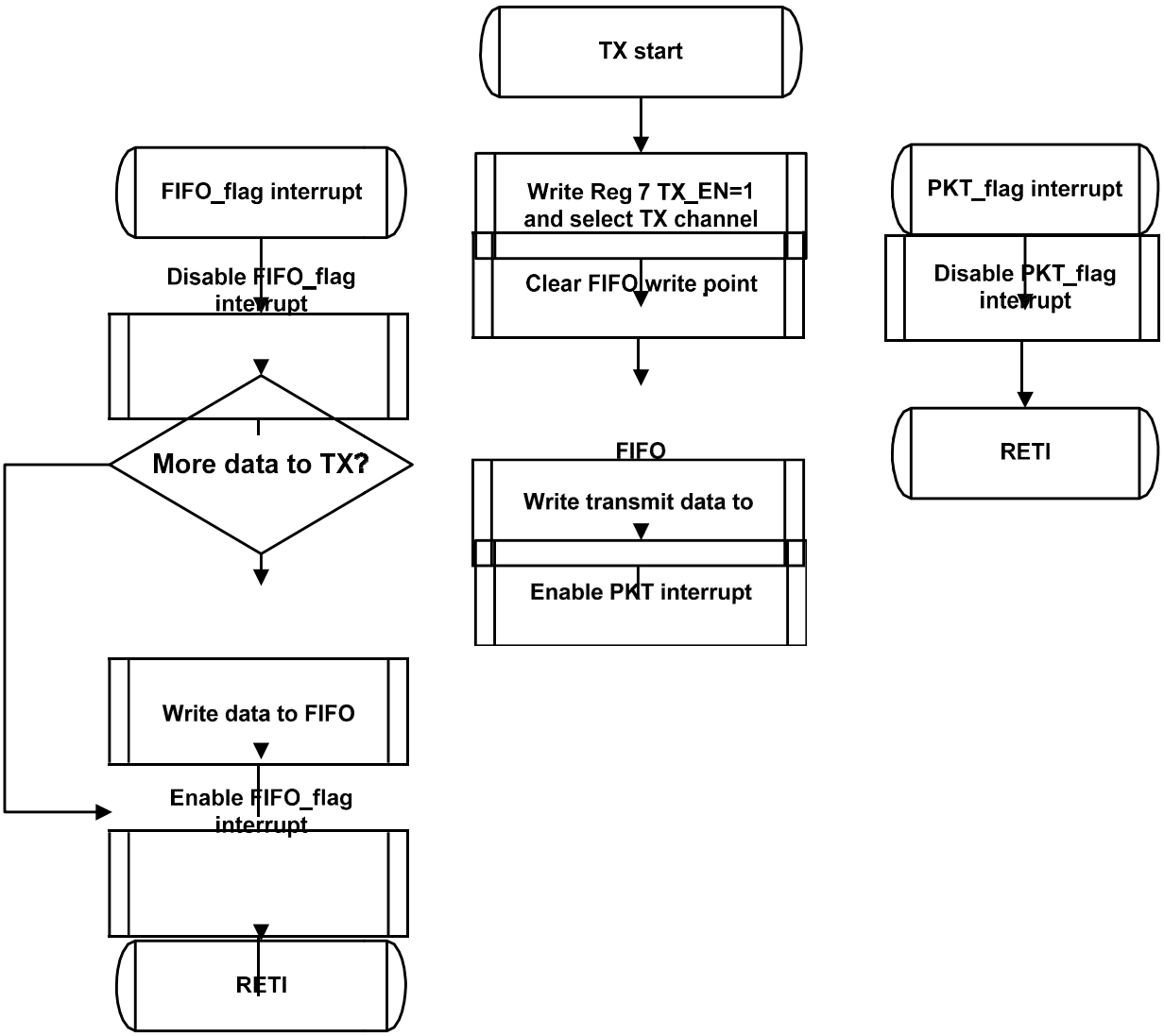


Figure 8. Example Tx packet flowchart

where FIFO and PKT flags are interrupt signals to MCU.



9.7. Receive Timing

Rx timing diagram is shown in figure below. When MCU writes Register 7[7]= 1 and selects receiving channel, HC24GB framer will turn on the receiver and wait while attempting to detect a valid syncword.

If valid syncword is found, the HC24GB framer will process packet automatically. When received packet processing is complete, HC24GB framer will set state to IDLE.

If received packet length is longer than 63 bytes, FIFO flag will go active, which means MCU must read out data from FIFO.

A valid syncword will not always be found, due to weak signal, multipath signal cancellation, devices out of range, etc. To accommodate such a condition and prevent lockup, the MCU/application should incorporate a receive timeout timer. In most applications, receive packets are expected to arrive within a defined time 'window'. If the packet does not arrive, the system can use either timer polling or timer-based interrupt to take corrective or alternative action.

Figure 9. Rx Timing Diagram when Register 41[13]=1 (Framer Handles Packet Length).

PKT and FIFO flags are Active High

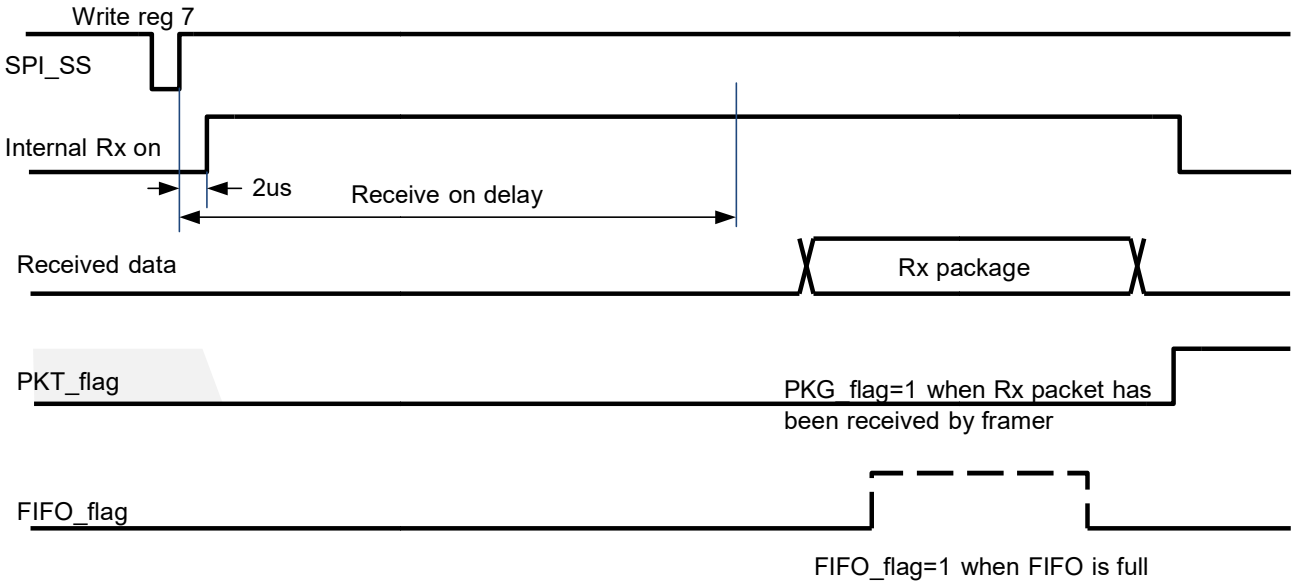
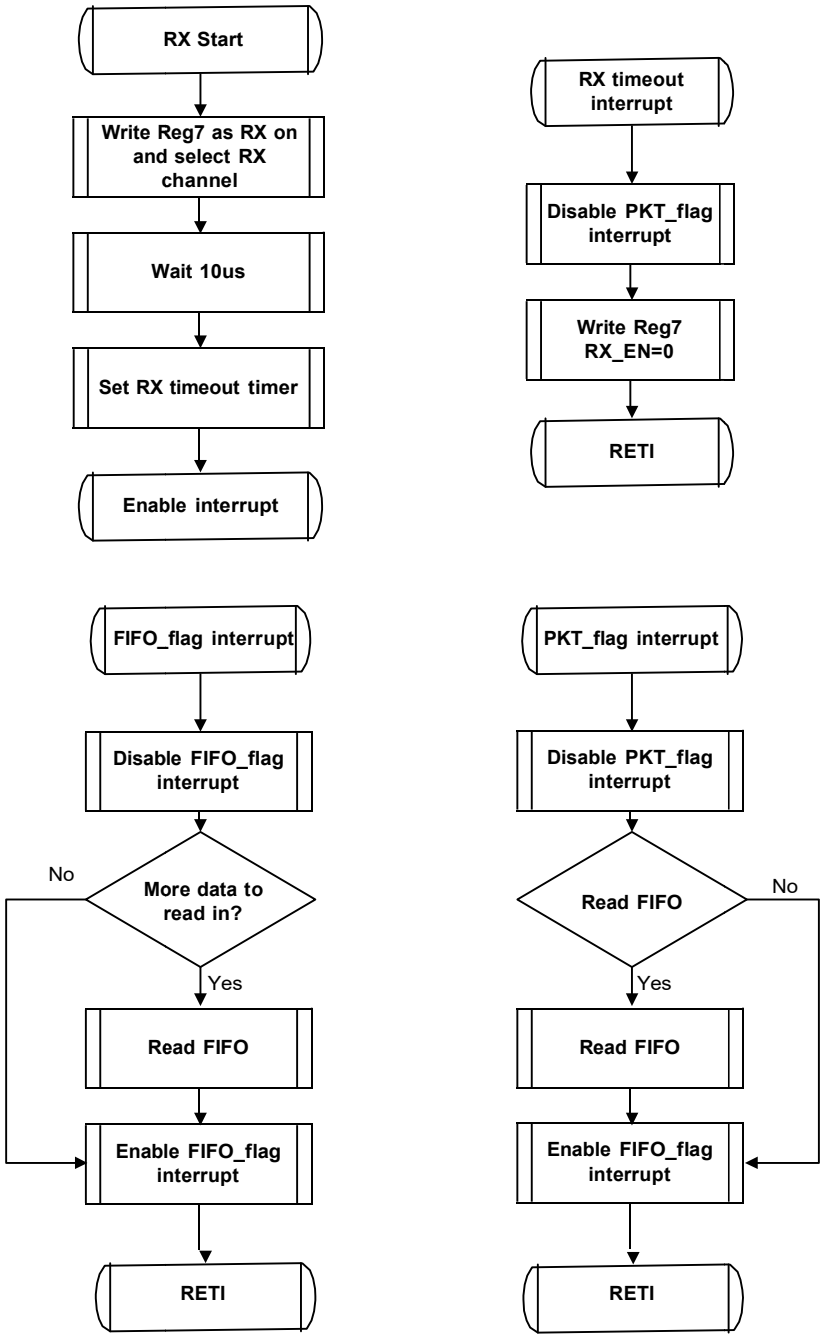


Figure 10. Example Rx packet flowchart

where FIFO and PKT flag signals interrupt MCU.



9.8. MCU/Application handles packet length

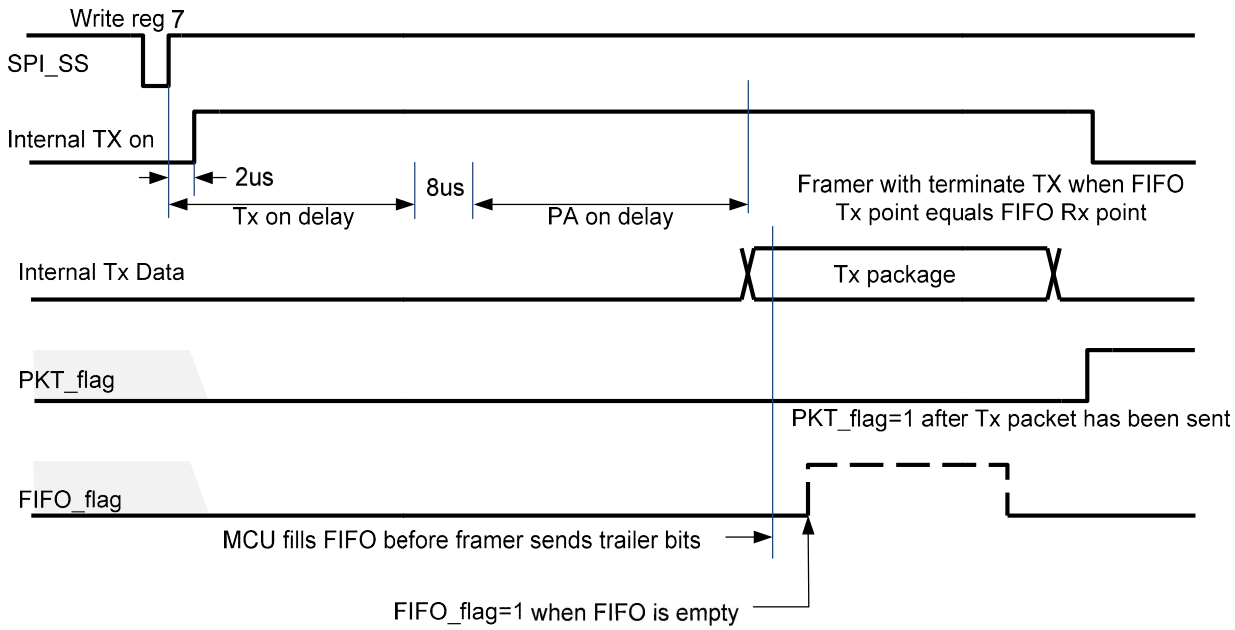
When Register 41[13]= 0, the 1st byte of the payload data has no special significance. Instead, packet length depends on Register 41[12].

9.8.1. FW_TERM_TX= 1

If Register 41[12] = 1, the HC24GB framer will continue to compare FIFO write point and FIFO read point during packet transmission. If MCU/application stops writing data to FIFO, the framer eventually detects that there is no data to send (FIFO empty), and HC24GB will exit cease transmission automatically. The timing diagram is shown in Figure below.

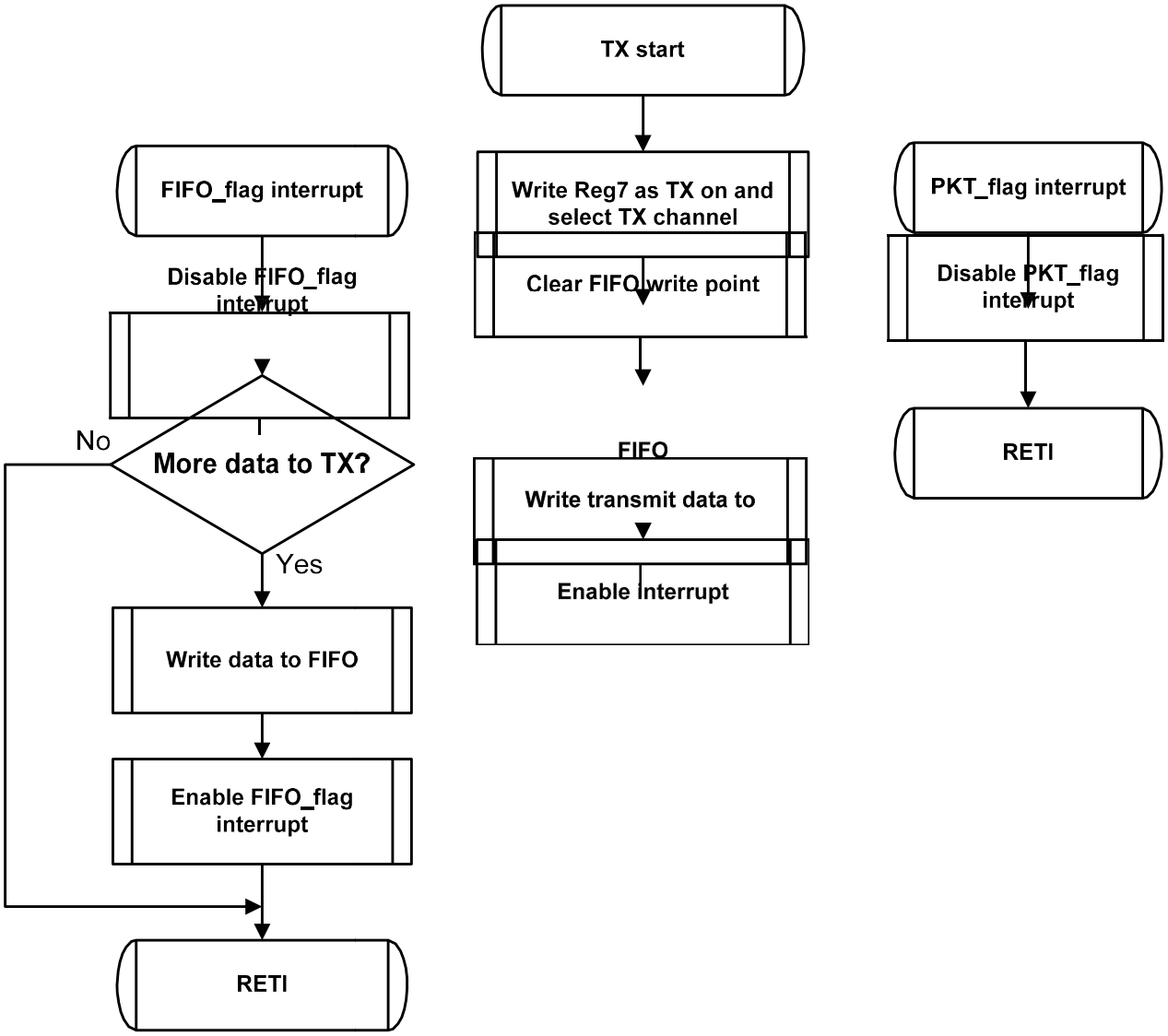
Figure 11. Tx timing when Register 41[13:12]= 'b01.

PKT and FIFO flags are set as active high.



Note: When Register 41[13] = 0 (MCU/application handles packet length), never let FIFO underflow or over flow. FIFO full/empty thresholds can be controlled via Register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value will depend on SPI speed, and speed at which MCU/application can stream the data into FIFO.

Figure 12. Example transmit flowcharts for Register 41[13:12]= 'b01 using interrupts for PKT and FIFO flags.

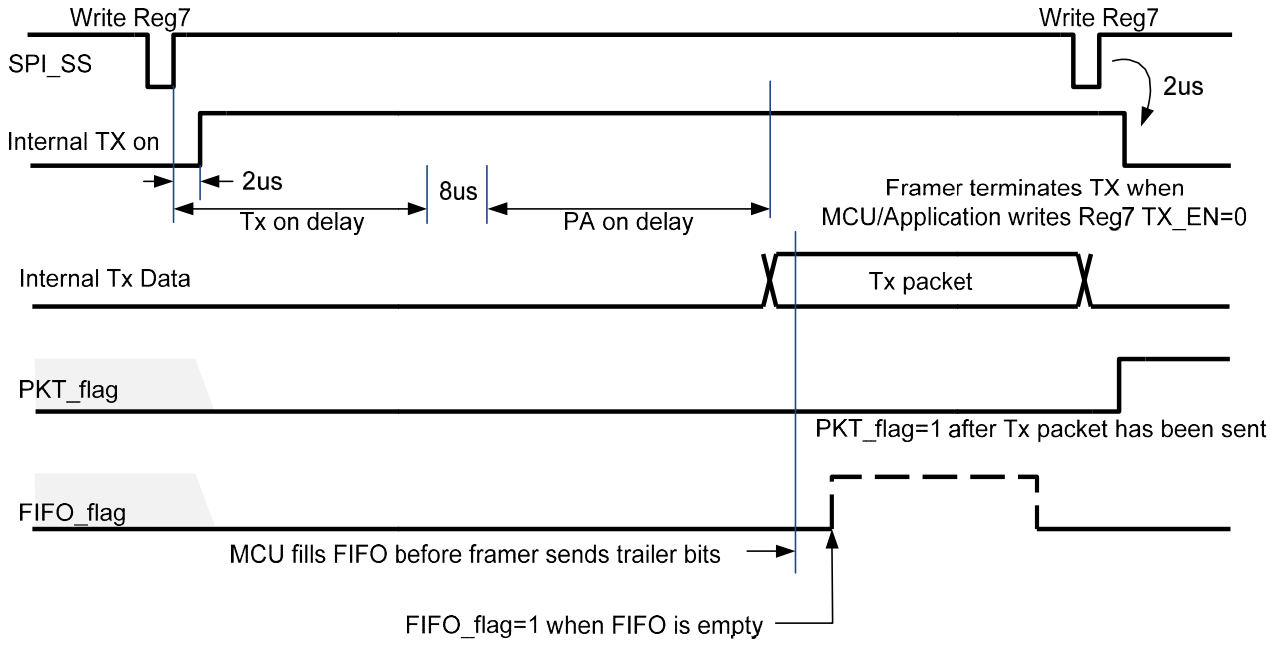


9.8.2. FW_TERM_TX= 0 (Transmit)

When Register 41[13:12] = ‘b00, the HC24GB framer does not stop packet transmission until MCU/application writes Register 7[8] TX_EN bit = 0. Packet transmission continues even if FIFO is empty. The timing diagram is shown in Figure below.

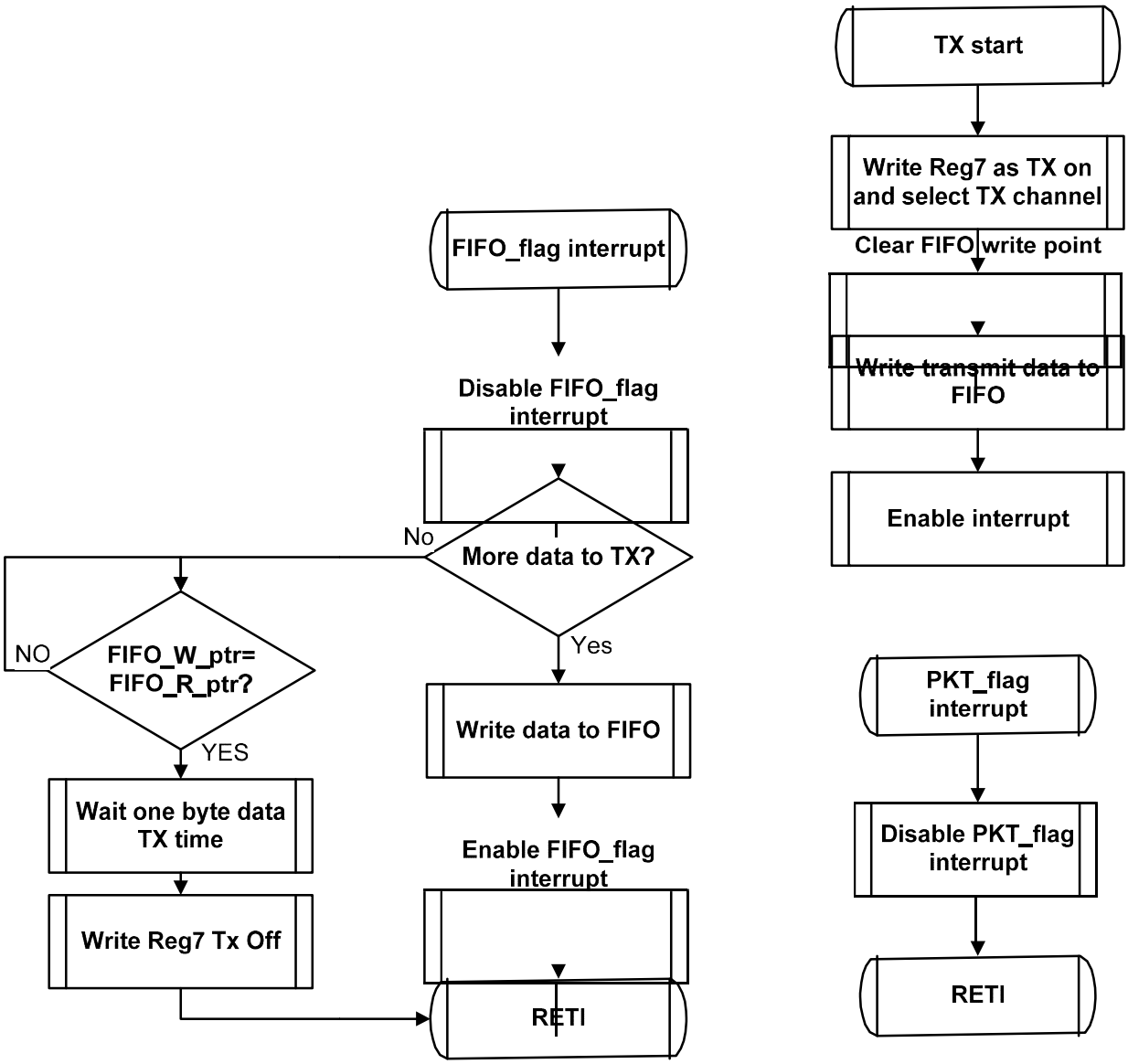
Figure 13. TX timing diagram when Register 41[13:12] = ‘b00.

PKT and FIFO flags are shown high active.



Note: When Register 41[13] = 0 (MCU/application handles packet length), never let FIFO underflow or over flow. FIFO full/empty thresholds can be controlled via Register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value will depend on SPI speed, and speed at which MCU/application can stream the data into FIFO.

Figure 14. Example Transmit flowcharts for Register 41[13:12]= ‘b00 using interrupts for PKT and FIFO flags.



9.8.3. FW_TERM_TX= 0 (Receive)

When Register 41[13] =0, packet reception starts when MCU/application writes Register 7[7] RX_EN = 1. At this time, the framer will automatically turn on the receiver to the frequency/channel specified in register 7. After waiting for the internal synthesizer and receiver delays to transpire, the framer circuitry of the LT8900 will begin searching the incoming signal for a syncword. When detected, it will set PKT flag active, then start to fill FIFO with receive data bytes. The PKT flag will remain active until MCU/application reads out the first byte of data from FIFO register. After MCU/application reads the first byte of receive data, PKT flag goes inactive until next Tx/Rx period.

With Register 41[13:12] = ‘b00 or ‘b01, the LT8900 framer will always need the MCU/application to write Register 7[7] to 0 to stop Rx state.

Rx timing diagram is shown in Figure below.

Figure 15. RX timing diagram when Register 41[13:12] = ‘b00 or ‘b01.

PKT_flag and FIFO_flag are active high.

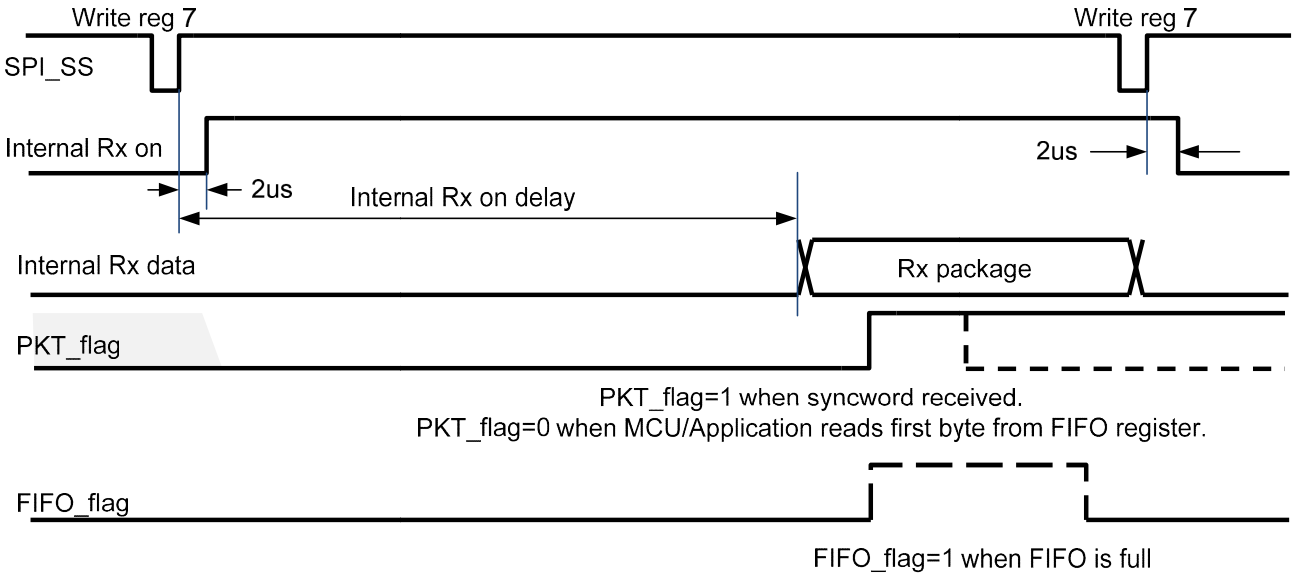
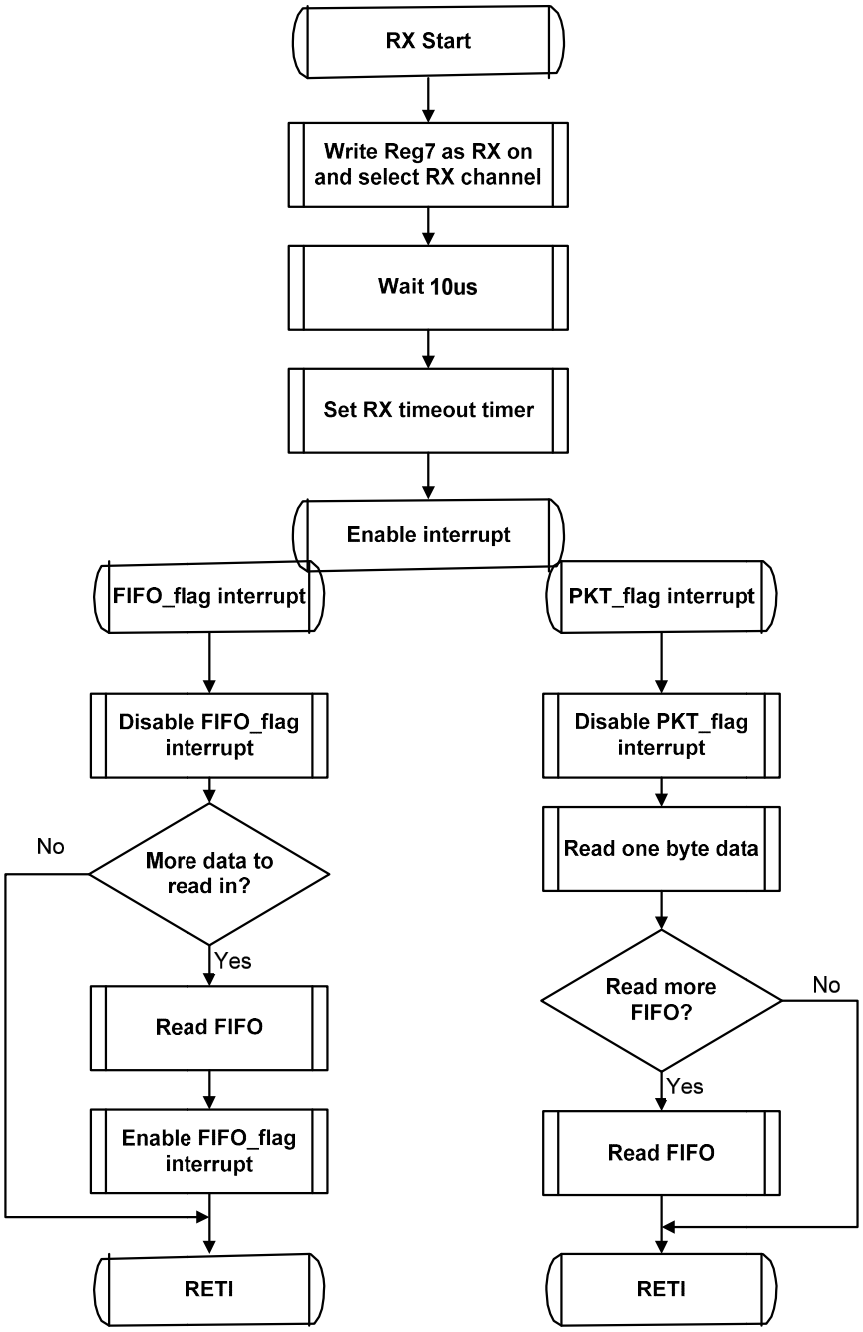
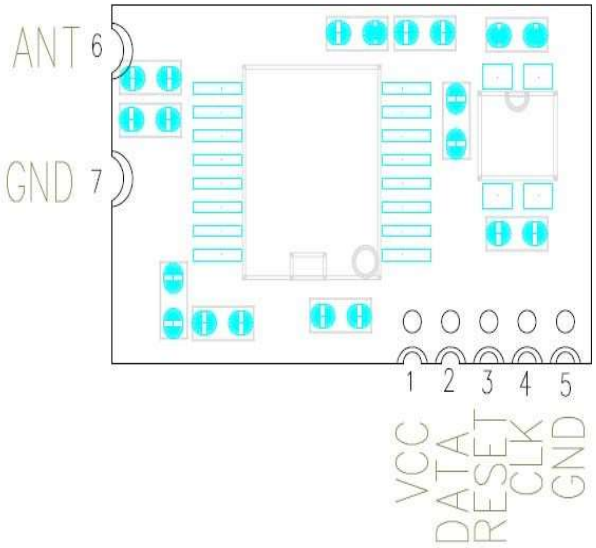


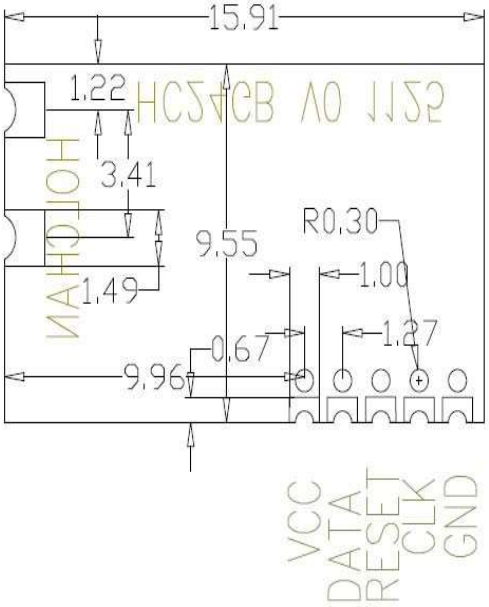
Figure 16. Example Receive flowcharts for Register 41[13:12]= ‘b00 or ‘b01 using interrupts for PKT and FIFO fla



10. Module Package Outline Drawing and picture

Unit: mm





11. Module Revisions

Rev 1.2 Mar 2014: The first release

12. Contact us:

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